Neuromorphic Hardware: A System Perspective

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1 Abstract

Neuromorphic computing has received great interest recently, promising to achieve the same efficiency as the human brain in solving complex, real-world problems. It is based on the idea of mimicking the basic elements of brains, neurons and synapses, in order to realize more efficient technical systems and to help in better understanding the biological counterpart ("understanding by building"). One of the visions of neuromorphic computing is to achieve human-level intelligence in a similar power budget as those 20 Watts estimated for the human brain.

When it comes to designing neuromorphic hardware systems, a key observation has long been driving the development: transistors in silicon have the same electrical conduction mechanism as ion channels in neurons if they are operated in the so-called subthreshold regime. Consequently, silicon neurons and synapses have been realized with subthreshold circuit techniques, and a great variety of hardware systems have been designed for diverse applications, always with the promise of ultra low power consumption due to the very low currents and voltages of transistors operated in that regime.

For a long time, the size and capabilities of neuromorphic hardware was quite limited, and demonstrations remained simple, despite a drive in the community to get ones hands dirty in real-world applications. Systems at a much larger scale in terms of number of neurons would be necessary to even start thinking about human-level performance. Only in the last few years, large-scale neuromorphic hardware systems have been developed and deployed, like IBM TrueNorth, the BrainScaleS wafer-scale system, Intel Loihi or SpiNNaker. Most of them break with several key postulates of neuromorphic hardware, which are, using transistors in the subthreshold regime, employing analog computation, avoiding clock signals via asynchronous operation, and getting around the von-Neumann bottleneck of classical computer systems by merging memory and processing. Still, these systems were able to outperform more wide-spread computing approaches like deep neural networks in terms of energy efficiency, while allowing to tackle much more complex computational tasks than any neuromorphic system before.

In my talk, I will sketch why a break with key postulates of neuromorphic hardware is sometimes instrumental when developing large-scale systems, and not too detrimental in other cases. I will describe how large-scale neuromorphic systems still follow a neuromorphic approach and how high energy efficiency can be achieved when being constrained by factors like robustness, stable operation and usability. Those factors start playing a dominant role when it comes to designing and successfully operating a system at large scale, as well as moving towards a commercial application.

As illustration, I will give insights into the design of the SpiNNaker2 system. Developed by the University of Manchester and Technische Universität Dresden since 2013, this neuromorphic many-core system is built for a system size of 10 million ARM microcontoller cores. It combines a slim, neuro-inspired communication fabric with dedicated hardware accelerators, making it an efficient and flexible platform for biological neural networks, but also deep neural networks and other highly parallel, sparse computing tasks.

Finally, I will give an outlook on potential future developments in neuromorphic hardware and how they link to recent trends in the field of artificial intelligence.

2 Short Bio

Johannes Partzsch is group leader at the chair of highly-parallel VLSI systems and neuromorphic circuits (HPSN) at Technische Universität Dresden. He obtained his PhD in 2014 at the same institution, focusing on connectivity in neuromorphic systems. His research interests include neuromorphic hardware and system development, as well as neural simulation, numerical function accelerators and edge AI hardware. He has contributed to the design of the BrainScaleS, Bionect, Titan and SpiNNaker2 neuromorphic hardware systems. He has been leading the ZEN project team winning first price in the innovation competition on energy-efficient AI systems by the German ministry of education and science in 2021. He is currently coordinating the construction of the SpiNNaker2 neuromorphic supercomputer 'SpiNNcloud' at TU Dresden.