Photonics Systems: Physical Layer to Scaled Architectures

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Computing platforms with increased parallelism at all scales:

Sun Niagara
8 cores
2005

Sony/Toshiba/IBM Cell
9 cores
2006

Intel Polaris
80 cores
2007

Tilera TILE-Gx100
100 cores
2009

NVIDIA TEGRA X1
256 GPUs
2016

Handheld
System-on-Chip

Embedded Systems

Data Centers
Supercomputing Performance

- Current World Top Supercomputers are Petascale:
  
  #1) TaihuLight (China)  Peak: 125 PetaFLOPs (PF)
  #2) Tianhe-2 (China)  55 PetaFLOPs (PF)
  #3) Titan (US)  27 PetaFLOPs (PF)

- Worldwide drive to reach Exascale in next few years
- Need a 10x improvement factor to Exascale
Supercomputing Performance

- CPU compute power is **decreasing**
  → Exploding parallelism
Data Movement Dominates—Energy
The Major Lag in Data Communications…

Top 10 Supercomputers computation capabilities over past 6 years:

- Vast increase in parallelism…but bandwidth is stagnated

- While system compute power grows by 23X
- Node I/O bandwidth increases by only < 3X

→ Data-movement is too expensive! ($ and Energy)
Mid 2000s: Silicon Photonics

Silicon-on-insulator (SOI) platform photonic building blocks:
High index contrast enables high confinement, low-loss propagation, virtually lossless bending
Silicon Photonics: all the parts

- Silicon as core material
  - High refractive index; high contrast; sub micron cross-section, small bend radius.

- Small footprint devices
  - 10 μm – 1 mm scale compared to cm-level scale for telecom

- Low power consumption
  - Can reach <1 pJ/bit per link

- Aggressive WDM platform
  - Bandwidth densities 1-2Tb/s pin IO

- Silicon wafer-scale CMOS
  - Integration, density scaling
  - CMOS fabrication tools
  - 2.5D and 3D platforms

The Photonic Opportunity for Data Movement

- Energy efficient, low-latency, high-bandwidth data interconnectivity is the core challenge to continued scalability across computing platforms
- Energy consumption completely dominated by costs of data movement
- Bandwidth taper from chip to system forces extreme locality

Reduce Energy Consumption

Eliminate Bandwidth Taper
Silicon Photonics for Computing

Exaflop-scale high-performance computing system

DRAM  CMPs 3DI Stack

Silicon Photonic Interconnection Network

Memory Stack

Seamless hierarchical photonic cross-layer communication to the chip

Photonic interconnects support inter-rack communications
Power requirements

- Today’s largest envelope: Tianhe-2 = 17MW; Sunway = 15MW
- Exascale at 100MW is maximal consideration: **10 GigaFLOP/Joule**
- 20MW total system power envelope preferred: **50 GigaFLOP/Joule**
Network energy requirements

End-to-end data movement energy budget:

- 10 Gigaflop/J, 10% of the envelope
- 10 Gigaflop/J, 15% of the envelope
- 50 Gigaflop/J, 10% of the envelope
- 50 Gigaflop/J, 15% of the envelope

Energy budget per bit (pJ):

- 100s of pJ to 10s pJ
- 10s of pJ to single pJs
- pJs to fJs!
Photonic Computing Architectures: Beyond Wires

Reconfigurable photonic switches

High density integration of WDM transceivers with CMOS

Data density and energy benefits

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>10 Gb/s * 100 wavelengths = 1Tb/s</td>
</tr>
<tr>
<td>Efficiency</td>
<td>~ 1pJ/bit (end-to-end)</td>
</tr>
</tbody>
</table>
Electronic Packet Switched Networks

Packet (electrical) switching

Input circuit

Output circuit

Xbar circuit

[Image of a busy urban intersection with heavy traffic]
Optics = Circuit Switching…

- Optical circuit switching: sets up link for data stream
- When a switch “turns,” no transmission can occur

• Streaming circuit data **cannot be slowed** when in motion
Consider Photonic Architecture for Computing: Dragonfly Network Topology

- Dragonfly provides balanced BW between every 2 groups
- More communication with neighboring groups
- Dragonfly provides balanced BW between every 2 groups
- Much more communication with neighboring groups
- More comm with neighboring groups

Huge Mismatch Between Topology Bandwidth and Workload Traffic
Flexfly: Enabling a Reconfigurable Dragonfly Through Silicon Photonics

- Flexible global bandwidth allocation for different applications
- *Optical Solution: reconfigure inter-group light on demand*
- Optical switching for *Bandwidth Steering*
- Significant Speedup with *low-radix Silicon Photonic switches*

Fixed Dragonfly

One of many Flexfly instances!

Insertion of multiple low-radix SiPh switches

Photonic FlexFly: Applications Speedup

GTC: 7x over MIN
1.8x over UGAL

Nekbone: 2x over MIN
1.4x over UGAL

LULESH: 5x over MIN
1.7x over UGAL

Optically Switched
8x8

32x32
Flexfly: Dragonfly Reconfigurable

- Flexfly can be implemented by optical switches of **reasonable** radices.

- Optical switch radix scales with the number of groups (e.g. 16 in reality).
- Number of optical switches reduced if they share same configuration and with WDM
32-node Flexfly Prototype

4 Groups Silicon Photonic Switch

Throughput (Gbps)

0 10 20 30

Time (s)

Flexfly
Dragonfly

2x throughput
Silicon Photonics Technology – toward Commercialization

**Fundamental Discoveries**
- low-loss, single-mode waveguiding
- optical coupling
- optical modulation via carrier injection

**Introduction of Innovative Devices**
- high-speed microring modulators and switches
- high-speed MZM modulators and switches
- arrayed waveguide gratings
- germanium photodetectors
- ultra low-loss waveguides and crossings
- hybrid silicon lasers

**Integration and Commercialization**
- Hybrid platforms
- Foundry and Design Services

**Timelines**
- 1990s
- 2000s
- 2010
- 2015+
The Integrated Photonics Manufacturing Institute’s Core Hubs - Albany

- 1.3M ft² facility
- cutting edge 300/450mm toolset
- 135k ft² of class 1 capable cleanroom
- processing capability span 65nm - 7nm

- years of proven silicon photonics results – multiple government & industry projects
- 300mm tools provide unprecedented quality photonics
- unmatched 3D stacking w/CMOS
- partnerships drive continuous revitalization investments
Market needs Common Manufacturing Technology Platforms to unfold its Potentials / Opportunities …

- Industry sets the pace: exploring technology potentials, revolutionizing the data and sensing market
  - Market is materializing
  - Stunning growth rates projected
  - It’s the technology of the future

- Scientific/Defense leverages industry pace: building on solid ground, adding uniquely required functionalities

Institute (Verticals) – KTMA’s Key Technology Manufacturing Areas

<table>
<thead>
<tr>
<th>Industry</th>
<th>DataCom / Telecom</th>
<th>Analog RF Applications</th>
<th>PIC Sensors</th>
<th>PIC Platform Technologies</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internet / Datacenters</td>
<td>CATV / Cellular</td>
<td>Spectroscopy</td>
<td>LIDAR / 3D Displays</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Increase</th>
<th>Capacity / Flexibility</th>
<th>Quality / Reliability</th>
<th>Sensitivity</th>
<th>Safety</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable</td>
<td>Internet Scaling</td>
<td>Subcarrier Applications</td>
<td>Environmental / Proactive Healthcare</td>
<td>3D Augmented Reality</td>
</tr>
</tbody>
</table>

| Decrease | Power / Cost | Cost | Healthcare Cost | Cost |

|-----------------------------|----------------------------------------|-----------------------------|------------------------|----------------------|

<table>
<thead>
<tr>
<th>Increase</th>
<th>Capacity / FLOPs</th>
<th>Bandwidth &amp; Reliability</th>
<th>Safety &amp; Health</th>
<th>Detection Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable</td>
<td>Reallocatable Bandwidth in Theater / Multiscale Modeling</td>
<td>Enhanced Capability</td>
<td>Warfighter</td>
<td>Augmented Reality</td>
</tr>
</tbody>
</table>

| Decrease | Power / Cost | Weight / Cost / Power | Cost | Cost |

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Holistic Integrated Photonic Manufacturing Technology Platforms

- Modular value chain – design, wafer fabrication, assembly, to packaging and test

- Core Manufacturing Locations
  - Analog Photonics, Massachusetts
  - SUNY Polytechnic Institute, New York
  - UCSB, California
  - SUNY Polytechnic Institute, New York
  - University of Rochester, New York
  - Columbia University, New York
  - MIT, Massachusetts

- Workforce Coordination
  - MIT, Massachusetts

- Electronic Photonic Design Automation
- Multi Project Wafer / Assembly
- Test, Assembly & Optical Packaging
- Inline Control & Test
- Education / Workforce Development
- Design / PDK
- 2.5D Interposer
- 3D ChipStack
- SiPh Wafer
- Parametrics / Functionality
- PCB
- Roadmap

Connecting the Physical World to Silicon – electromagnetics / photonics / fluidics
Thank you